DPD02 – ADAPTIVE DIGITAL PRE-DISTORTION

OVERVIEW

Digital Pre-distortion (DPD) has become the industry standard for linearity improvement in digital amplifier designs. By measuring transmitter distortion and applying an inverse correction at the digital modulator output, adaptive pre-distortion provides predictable transmitter linearity, low out of band emissions, improved efficiency and lower overall amplifier cost.

The Affarii DPD02 predistortion processor is a third generation adaptive pre-distortion engine designed for linearization of Class-AB and Doherty amplifiers based on LDMOS and GaN transistors.

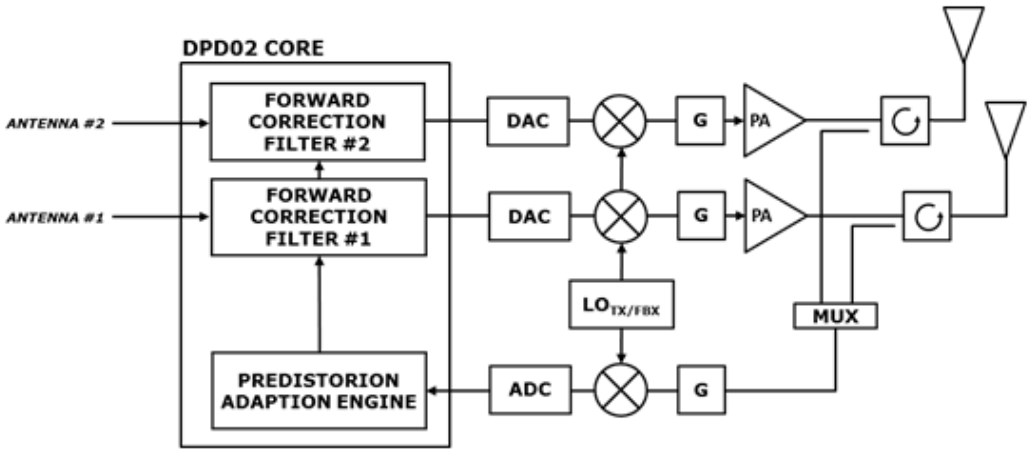
The DPD02 core includes configurable memory compensation for both thermal and reactive memory effects present in typical amplifier designs. This allows the predistortion to achieve up to 30dB of ACP correction when implementing multi-carrier High Power Amplifiers (HPA) at peak power saturation.

The DPD02 core includes support for Multi-Output transmit configurations (MIMO) allowing correction of up to four transmit antennas to be slaved to a single master adaption engine using hardware adaption acceleration.

FEATURES

- Typical 20-30dB ACLR Correction.
- Reactive Memory Compensation.
- 20-50MHz Bandwidth (100-250Msps).
- AQM and DC Feed-through Correction.
- Class-AB & Doherty Support.
- Multi-Antenna (MIMO) Capable.
- Adaption Hardware Acceleration.
- FDD and TDD Operation Modes.

BLOCK DIAGRAM



DESCRIPTION

The DPD02 digital predistortion processor is an IP firmware block target for application in low cost FPGA fabric and ASIC designs.

The DPD02 IP core has a modulator design that consists of a Forward Correction Filter (FCF) element for each transmit antenna amplifier to be linearised, and a common Predistortion Adaption Engine (PAE) that tracks PA characteristic variations and updates the FCF parameters.

The correction filter for each antenna includes a predistortion modulator (PDM), transmit equalizer (EQU) and quadrature modulator correction (QMC) block. An optional rate conversion filter (RCF) is also available to interpolate the input sample data to the output oversample rate required for pre-distortion operation.

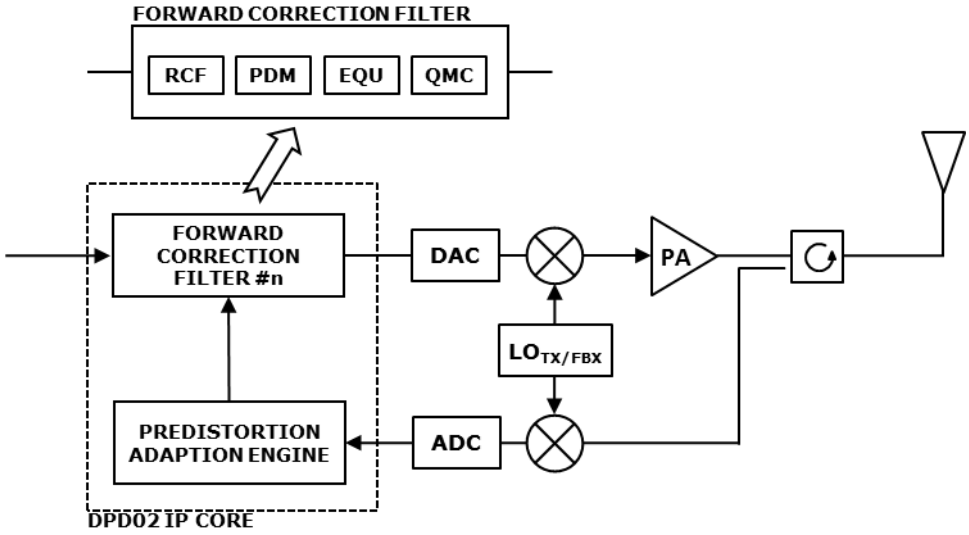


Figure 1: DPD02 - Internal Block Architecture

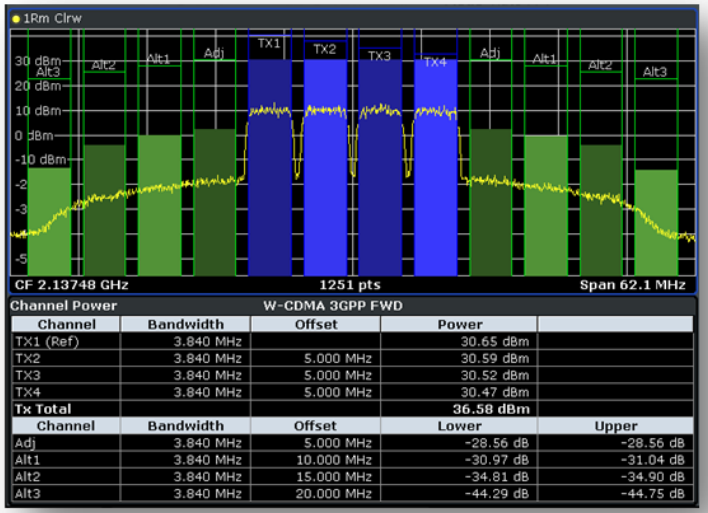
The inclusion of quadrature modulation correction allows the IP core to be used with wide band direct conversion transmit architectures. With a good board layout real time automatic suppression of the analog quadrature modulator carrier feed through and IQ imbalance exceeding 65dBc can be achieved without prior calibration.

The DPD02 processor supports multi-output transmitters (MIMO) by allowing up to four correction filters (FCF) for independent antenna elements to be slaved to a single master Predistortion Adaption Engine (PAE).

EXAMPLE:

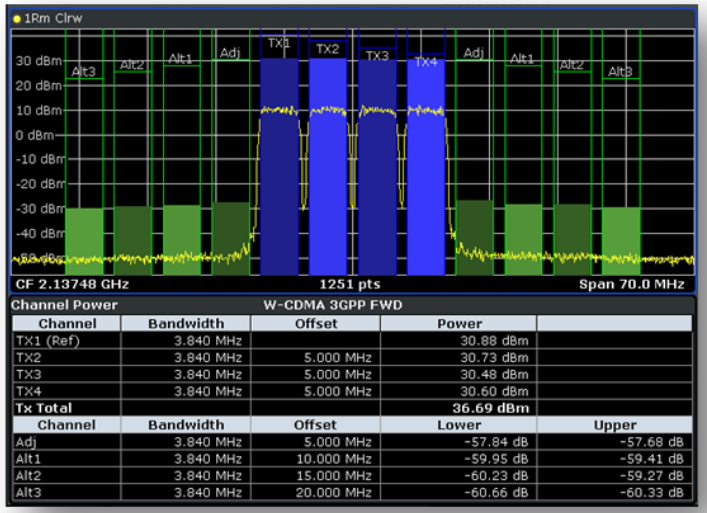
BROADBAND AMPLIFIER (700-2500MHz)

- PA operated at 2.7dB compression point with initial -31dBc ACP.
- Supports 20MHz WCDMA waveform with 1FA to 4FA dynamically switched.
- ACP correction is >27dBc using Memory Effect Linearization (“1111” shown)



Channel Power W-CDMA 3GPP FWD

Channel	Bandwidth	Offset	Power	
TX1 (Ref)	3.840 MHz		30.65 dBm	
TX2	3.840 MHz	5.000 MHz	30.59 dBm	
TX3	3.840 MHz	5.000 MHz	30.52 dBm	
TX4	3.840 MHz	5.000 MHz	30.47 dBm	
Tx Total			**36.58 dBm**	
Channel	**Bandwidth**	**Offset**	**Lower**	**Upper**
Adj	3.840 MHz	5.000 MHz	-28.56 dB	-28.56 dB
Alt1	3.840 MHz	10.000 MHz	-30.97 dB	-31.04 dB
Alt2	3.840 MHz	15.000 MHz	-34.81 dB	-34.90 dB
Alt3	3.840 MHz	20.000 MHz	-44.29 dB	-44.75 dB



Channel Power W-CDMA 3GPP FWD

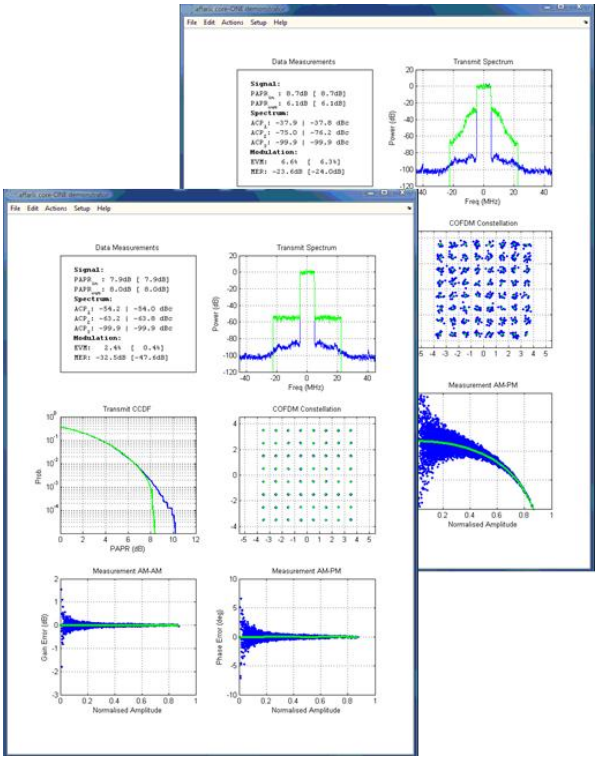
Channel	Bandwidth	Offset	Power	
TX1 (Ref)	3.840 MHz		30.88 dBm	
TX2	3.840 MHz	5.000 MHz	30.73 dBm	
TX3	3.840 MHz	5.000 MHz	30.48 dBm	
TX4	3.840 MHz	5.000 MHz	30.60 dBm	
Tx Total			**36.69 dBm**	
Channel	**Bandwidth**	**Offset**	**Lower**	**Upper**
Adj	3.840 MHz	5.000 MHz	-57.84 dB	-57.68 dB
Alt1	3.840 MHz	10.000 MHz	-59.95 dB	-59.41 dB
Alt2	3.840 MHz	15.000 MHz	-60.23 dB	-59.27 dB
Alt3	3.840 MHz	20.000 MHz	-60.66 dB	-60.33 dB

TOOL SUPPORT

The pre-distortion core is supported with comprehensive PC based analysis tools to assist in amplifier design and performance analysis.

Analysis tool include advanced visualisation in the MATLAB environment with USB based In Circuit Evaluation (ICE) tools that provide PA compression, AM-AM, AM-PM and equalisation characteristic data.

Conformance test signal generation and analysis software complaint with 3GPP TS25.141 (WCDMA) and TS36.141 (LTE) are available for both development and production test environments.



PERFORMANCE

The performance of all DPD designs varies depending on RF amplifier design architecture (Class-AB, Doherty), power output, signal bandwidth and RF layout and power supply design.

The DPD02 core has been verified with RF Amplifier designs based on Class-AB and Doherty architectures having output powers ranging from 4W to 1KW and using GaN, GaAS and LDMOS transistor types. For information on specific applications please contact **sales@affarii.com**.

AVAILABILITY

The DPD02 predistortion processor is available as a standalone IP block for Altera and Lattice FPGAs or as part of the digitalTRX solution set. For further information please contact **sales@affarii.com**.

Contact Information:

Affarii Technologies Limited
St John's Innovation Centre,
Cowley Road,
Cambridge, CB4 0WS
UNITED KINGDOM.

Web: www.affarii.com
Email: sales@affarii.com
Tel: +44-8456-801049
Fax: +44-8456-801059

Legal Notice:

The information presented is subject to change without notice. Customers are responsible for their own product design and for verifying the suitability of the design products for their end application. When implementing products customers should ensure adequate design margins and operating safeguards are provided.

Affarii Technologies Limited reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time, and to discontinue any product or service without notice.